REMARKS

Claims 1-22 are pending in the present application, and were each rejected.

Claims 1-22 remain in the present application.

Reconsideration of the claims is respectfully requested.

CLAIM REJECTIONS -- 35 U.S.C. §102

Claims 1-22 were rejected as anticipated by *Lipman et al.* (USP 6,192,051, hereinafter "Lipman"). These rejections are traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

Independent claims 1 and 11 each require "a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit". This feature is not taught or suggested by Lipman.

While Lipman's Figure 11 does show that IP address bits [31:16] provide the index of an entry in the level-1 tree 150 (col. 15, lines 59-61), the output "Next Tree Index" (the "NT pointer") is

not used to "access[] an address table in a second memory circuit" where the second memory circuit is one of the "M pipelined memory circuits", as claimed in Claims 1 and 11. Instead, the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

Figure 11 shows that the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67), and nothing teaches or suggests that the forwarding table . That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

The Examiner now indicates that he believes that element 144 portion "128.63" satisfies the claimed "first portion of said first received address". On the contrary, Lipman describes that "A portion of the level 1 tree 140 is shown in FIG. 7, including locations 128.63 through 128.68." *Col. 10, lines 59-60.* Applicant assumes that this is a typographic error in the patent, and the reference to "140" should be to "144".

The Examiner also indicates that Lipman's next tree table 152 is the claimed "address table in the second memory circuit". Of course, by combining element 144 from Figure 7 and element 152

of Figure 11, the Examiner is unable to show at all that there are any pipelined memory circuits, as these two figures do not show any common elements interrelating. Figure 11 is describing a compressed tree, Figure 7 is describing an uncompressed tree, and these do not interrelate.

In fact, though Lipman shows multiple tables that point to each other, nothing in Lipman's description teaches or suggests a lookup circuit comprising "M pipelined memory circuits" as claimed. The Examiner's statement that "these memory circuits are 'pipelined' in that they each point to another circuit" is not persuasive. Those of skill in the art recognize that a "pipeline" is a series of elements each connected so that the output of one element is an input of the next element. See, for example, Figure 3 of the present application, where the output of each pipelined SRAM is an input to the next one in series. Lipman does not appear to teach or suggest such a pipeline at all, much less pipelined memory circuits.

The Examiner refers to Lipman's Figure 7 for "pipelined memory circuits", but this figure shows a diagram of a data structure, not memory circuits. If the Examiner is intending to imply that the actual semiconductor circuits that comprise each bit/cell of a memory are the "memory circuits", then the Examiner will surely recognize that these are not typically pipelined, and Lipman certainly doesn't teach any such pipelining. Lipman doesn't teach series connections or pipelining at all.

As such, Lipman does not anticipate independent claims 1 or 11, or their respective dependent claims 2-10 and 12-20.

Claim 21 requires that the output from the address table in the first memory circuit is a first address pointer that indexes a start of an address table in a second memory circuit. Claims 2 and 12 include similar limitations. These features are not taught or suggested by Lipman.

As described above, the output of the level-1 tree 150 (the NT pointer) is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). Lipman also describes that the base of the level-2 next tree table 152 is pointed to by the level 2 pointer 218 from the level pointer block 210. As such, it is clear that the NT pointer does not index a start of the address table in the second memory circuit, as claimed. As such, it is clear that Lipman also does not teach or suggest the features of claims 2, 12, or independent claim 21. Claim 21 also requires M pipelined memory circuits, not taught or suggested by Lipman. Lipman similarly does not teach or suggest the features of dependent claim 22. These rejections are traversed.

Other distinctions remain, but those described above are sufficient to demonstrate that Lipman does not anticipate claims 1-22. All rejections are traversed.

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SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of the pending claims and that this application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@munckbutrus.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS P.C.

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